This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1.-2. (Canceled)

3. (Currently amended) A ~~flow analyzer collecting~~system configured to collect data with substantially zero dead time ~~for at least one event~~, comprising:

a flow analyzer configured to collect data for events in successive sampling periods with substantially zero dead time between the successive sampling periods;

at least one buffer having a plurality of data storage areas, ~~that are~~wherein the at least one buffer is adapted to receive ~~and store incoming~~ the data from ~~a plurality of sampling periods~~ for ~~the at least one event collected by~~ said flow analyzer and to store the data for each of the successive sampling periods in different data storage areas with substantially zero dead time between storage of the data in the different data storage areas, and wherein said at least one buffer ~~including previously stored data from a sample period preceding a current time of the receipt and the storage of the data and including~~comprises an addressable range of the plurality of data storage areas to go sufficiently backward in the ~~plurality of~~successive sampling periods; and

at least one processor connected to said at least one buffer, ~~receiving~~ wherein the processor is adapted to receive and process the data from ~~the at least one of~~ the plurality of data storage areas of said at least one buffer~~, and said flow analyzer collecting and processing the data from the at least one event with substantially zero dead time by reading from said at least one buffer the previously stored data from the sampling period preceding the current time of the plurality of sampling periods~~.

4. (Original) The flow analyzer of claim 3, where the flow analyzer is a flow cytometer.

5. (Currently amended) A ~~flow analyzer collecting~~system configured to collect data with substantially zero dead time ~~for at least one event~~, comprising:

a flow analyzer configured to collect data for events in successive sampling periods with substantially zero dead time between the successive sampling periods;

at least one buffer means for having a plurality of data storage areas, wherein the at least one buffer means is ~~that are~~ adapted to receive ~~and store incoming~~ the data from ~~a plurality of sampling periods for the at least one event collected by said~~the flow analyzer and to store the data for each of the successive

sampling periods in different data storage areas with substantially zero dead time between storage of the data in the different data storage areas, and wherein said at least one buffer means ~~for including previously stored data from a sample period preceding a current time of the receipt and the storage of the data and including~~comprises an addressable range of the plurality of data storage areas to go sufficiently backward in the ~~plurality of~~successive sampling periods; and

at least one processor ~~for receiving~~adapted to receive and process the data from ~~the at least one of~~ the plurality of data storage areas of said at least one buffer means~~, and said flow analyzer collecting and processing the data from the at least one event with substantially zero dead time by reading from said at least one buffer means the previously stored data from the sampling period preceding the current time of the plurality of sampling periods~~.

6. (Original) The flow analyzer of claim 5, where the flow analyzer is a flow cytometer.

7. (New) A system configured to collect data with substantially zero dead time, comprising:

a flow analyzer configured to collect data during successive sampling periods with substantially zero dead time between the successive sampling periods;

an addressable buffer comprising data storage areas, wherein the addressable buffer is configured to store the data for each of the successive sampling periods in different data storage areas with substantially zero dead time between storage of the data in the different data storage areas; and

a processor configured to process the data in the different data storage areas.

8. (New) The system of claim 7, wherein the processor is further configured to process the data in the different data storage areas at a rate that is different than a rate at which the data is stored in the different data storage areas.

9. (New) The system of claim 7, wherein the processor is further configured to process the data in the different data storage areas after the data has been stored in the different data storage areas for a time longer than a longest possible time for an event.

10. (New) The system of claim 7, wherein the processor is further configured to process the data in the different data storage areas at a rate that is determined based on a signal-to-noise ratio of the data in the different data storage areas.

11. (New) The system of claim 7, wherein the addressable buffer further comprises a number of the data storage areas such that a predetermined amount of the data backward in time is available for re-processing by the processor.

12. (New) The system of claim 7, wherein the addressable buffer is a circular buffer.

13. (New) The system of claim 7, wherein the addressable buffer is a cascading buffer.

14. (New) The system of claim 7, wherein the addressable buffer is a First In-First Out buffer coupled to a backward cache.

15. (New) The system of claim 7, wherein one or more parameters of the flow analyzer, the addressable buffer, the processor, or some combination thereof are user specified.

16. (New) The system of claim 7, wherein the data storage areas are linked in an order such that the data for the successive sampling periods is stored in the data storage areas in the order in which the data storage areas are linked.

17. (New) The system of claim 7, further comprising a pointer configured to direct the storage of the data in the addressable buffer.

18. (New) The system of claim 7, further comprising an additional processor configured to direct the storage of the data in the addressable buffer.

19. (New) The system of claim 7, further comprising a field programmable gate array configured to direct the storage of the data in the addressable buffer.

20. (New) The system of claim 7, further comprising a pointer configured to direct processing of the data by the processor.

21. (New) The system of claim 7, further comprising an additional processor configured to process the data in the different data storage areas.

22. (New) The system of claim 7, wherein the processor is further configured to process the data stored in a series of the different data storage areas as being part of one event.

23. (New) The system of claim 7, wherein the data for each of the successive sampling periods comprises data from a plurality of channels of the flow analyzer.

24. (New) A method for collecting data with substantially zero dead time, comprising:

collecting data with a flow analyzer during successive sampling periods with substantially zero dead time between the successive sampling periods;

storing the data for each of the successive sampling periods in different data storage areas with substantially zero dead time between storage of the data in the different data storage areas; and

processing the data in the different data storage areas.